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EXAMINER	
CRAIG, DWIN M	
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8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/475,717	Applicant(s) NARDIN ET AL.
	Examiner Dwin M Craig	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-25-2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *2,7 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8-18, 20* is/are rejected.

7)☒ Claim(s) *19 and 21-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 2, 7 and 13 have been withdrawn from consideration as per Applicant's request. Claims 1, 3, 4, 8, 10, 14, 15 and 17 have been presented for reconsideration in light of Applicants amended specification. Claims 18-27 are new Claims that are being presented for consideration in light of Applicants amended specification. Claims 5, 6, 9, 11, 12 and 16 are presented for reconsideration in light of Applicants amended specification. After reconsideration Claims 1, 3-6, 8-12, 14-18 and 20 have been rejected. Claims 19, 21, 22, 23, 24, 25, 26 and 27 have been objected to because they are based on rejected base claims.

Response to Arguments

2.

2.1 Regarding Applicant's submission of amended drawings;

The Examiner respectfully asserts that no amended drawings have been presented at this time, therefore; this application has been filed with informal drawings which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed.

2.2 Regarding Applicant's response to Examiners rejections of Claims 1-17 under 35 U.S.C. § 102;

Applicant has asserted that;

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing Richardson v. Suzuki Motor Co., 868 F.2d 1226 (Fed. Cir. 1989)). Amended independent claim 1 now recites in pertinent part, "each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated ...." Applicants submit that Rajgopal fails to disclose simulating a domino logic circuit after any domino logic circuit feeding into its inputs has been simulated. Rajgopal is directed towards "a method of estimating power use by

a proposed electronic system design before the design is completed..." Rajgopal col. 2, lines 15-17.

In particular, Rajgopal discloses:

The input activity factor of blocks downstream from a domino block is changed as a result of the upstream domino blocks. The logic simulator does not correct these downstream blocks for the effect of the upstream use of domino blocks. Therefore, the AF values of the downstream blocks may be corrected at block 68 to account for the effect of the upstream domino blocks.

Rajgopal col. 4, lines 14-21 (Emphasis added).

Thus, Rajgopal discloses a simulator that does not correct downstream blocks for the effect of the upstream use of domino blocks. Applicant's claimed invention addresses this simulation problem by simulating each domino logic circuit after any domino logic circuit feeding into a domino logic circuit has been simulated. Rajgopal fails to disclose ordering the simulation of domino logic circuits as claimed by claim 1.

Examiner asserts that the *Rajgopal* reference does not disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed therefore the Examiner finds the Applicant's arguments to be persuasive, in regards to the *Rajgopal* reference and withdraws the 35 U.S.C.§ 102 rejection of amended Claims 1-17.

Applicant has asserted that;

Heikes also fails to anticipate amended claim 1. In particular, Heikes is directed towards "a system and method for performing precharge timing verification on a logic circuit..."and "determining the longest precharge path in the logic circuit." Heikes Abstract. However, Heikes fails to disclose simulating a domino logic circuit after any domino logic circuit feeding into it has been simulated. Consequently, each and every element of claim 1 is not found in Rajgopal or Heikes. Accordingly, Applicants respectfully request that the instant § 102(e) rejections of claim 1 be withdrawn. Amended independent claims 4, 10, 15, and 17 all now recite in pertinent parts, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list ...." Furthermore, these claims recite in pertinent parts, "simulating each domino logic circuit according to the ordered list." As discussed above, Applicants submit that both Rajgopal and Heikes fail to disclose simulating an ordered list that positions all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit. Accordingly, Applicants respectfully request that the instant § 102(e) rejections of claims 4, 10, 15, and 17 be withdrawn.

The Examiner asserts that applicants arguments regarding the *Heikes* reference is persuasive and that the *Heikes* reference does not expressly disclose using an ordered list and withdraws the 35 U.S.C. 103 rejection of Claims 4, 10, 15 and 17.

2.3 Regarding Applicant's response to the 35 U.S.C. § 103 rejections of Applicant's amended claims;

Applicant asserts that;

Claim 1 stands rejected under 35 U. S. C. § 103(a) as being unpatentable over U. S. Patent No.: 6,040,716 to Bosshart ("Bosshart") in view of Heikes. To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. M.P.E.P § 2143.03 (citing In re Royka, 490 F.2d 981).

Amended independent claim 1 now recites in pertinent part, "each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated ...." Neither Bosshart nor Heikes disclose, teach, or fairly suggest a method of simulating a domino logic circuit after any domino logic circuit feeding into it is simulated. Therefore, the combination of Bosshart and Heikes fail to teach or suggest each element of claim 1 as required Applicants note that some of the limitations of cancelled claim 2 have been moved into independent claim 1. Cancelled claim 2 stood rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.: 5,815,687 to Masleid et al. ("Masleid") in view of Heikes and in further view of Rajgopal. In support of this rejection the Examiner stated, "the Masleid et al. reference discloses simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated..." Applicants respectfully disagree. In particular, Masleid is directed to an "apparatus for and method of testing CMOS domino logic circuits in which pre-charge validation and functional evaluation are separated." Masleid col. 3, lines 6-8. However, Masleid, Heikes and Rajgopal, either alone or in combination, fail to disclose, teach, or fairly suggest a method of simulating a domino logic circuit after any domino logic circuit feeding into it has been simulated. Accordingly, Applicants respectfully request the instant § 103(a) rejection of claim 1 be withdrawn.

The Examiner asserts that the *Maslied et al.* reference discloses the following ***(Col. 4 Lines 49-55)*** "It should be understood that, while a four-phase domino logic circuit is shown, the invention is applicable to any number of stages or phases where each subsequent stage performs

its evaluation based on a previous evaluation, and in the final stage, an output being provided indicative of the validation of the precharge circuits in all stages." The preceding section taken from the *Maslied et al.* reference clearly discloses the dependence of each stages simulation and validation being based on the evaluation of the previous stage. The Examiner finds Applicant's arguments unpersuasive and therefore the Examiner asserts that the *Maslied et al.* reference does teach the limitations previously inclusive of Claim 2. However, due to the addition of the new limitations to amended Claim 1, regarding the need for an ordered list, the old 35 U.S.C. 103 rejection of what is now Claim 1 are withdrawn.

Claims 4-9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bosshart in view of Heikes and in further view of Rajgopal. Amended independent claim 4 now recites in pertinent part, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list ...." As discussed above, Bosshart, Heikes, and Rajgopal, either alone or in combination, fail to disclose, teach, or fairly suggest an ordered list positioning all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit. Consequently, Applicants respectfully request that the instant §103(a) rejection of claim 4 be withdrawn. Claims 10-16 stand rejected under 35 U.S.C. ,§§' 103(a) as being unpatentable over U.S. Patent No.: 5,825,673 to Watanabe ("Watanabe") in view of Rajgopal.

Amended independent claims 10 and 15 recite in pertinent parts, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list ...." The Examiner stated in the Office Action mailed September 3, 2002 that, "the Watanabe reference does not expressly disclose simulating each domino circuit, scheduling of the domino circuits in an ordered list such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino circuit." As discussed above in connection with the §102(e) rejection of claim 1, Applicants submit that Raj gopal also fails to disclose, teach, or fairly suggest an ordered list positioning all domino logic circuits feeding into another domino logic circuit before the another domino logic circuit in the ordered list. Accordingly, since each element of claims 10 and 15 are not taught or suggested by the combination of Watanabe and Rajgopal, Applicants request that the instant §103(a) rejections be withdrawn.

The Examiner asserts that the Applicant's arguments are persuasive in that the references sited do not teach the limitation of the ordered list, however the Examiner asserts that the references sited do teach the limitations recited in the previous versions of Claims 10 and 15. However in view of Applicant's amended claim language the previous 35 U.S.C. 103 rejection of Claims 10 and 15 are withdrawn.

Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Masleid in view of Heikes and in further view of Rajgopal. Amended independent claim 17 recites in pertinent part, "the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list ...." As discussed above in connection with claim 1, the combination of Masleid, Heikes and Raj gopal fails to teach or suggest every element of amended claim 17. Accordingly, Applicants respectfully request the instant § 103(a) rejection be withdrawn.

The Examiner asserts that the Applicant's arguments are persuasive in that the references sited do not teach the limitation of the ordered list, however the Examiner asserts that the references sited do teach the limitations recited in the previous versions of Claim 17. However in view of Applicant's amended claim language the previous 35 U.S.C. 103 rejection of Claim 17 is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3, 4, 5, 6, 8 and 9** are rejected under **35 U.S.C. 103(e)** as being unpatentable over **Rajgopal et al. U.S. Patent 6,363,515** in view of **Beausang U.S. Patent 5,828,579.**

3.1 As regards independent **Claims 1 and 4** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and Col. 4 Lines 1-22),** and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation to combine)* the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

3.2 As regards **Claim 3** the *Rajgopal et al.* reference discloses simulating each domino logic circuit including the simulated results of circuits coupled to the inputs of the domino logic circuit **(Col. 3 Lines 58-67, Col. 4 Lines 1-8).**

3.3 As regards **Claim 5** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

3.4 As regards **Claim 6** the *Rajgopal et al.* reference discloses a reporting of the results of the simulation, **(Figure 1, Col. 7 Lines 26-39).**

3.5 As regards **Claim 8** the *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item 22),** an ordered list **(Figure 6 Item 72, Figure 5 and Figure 4)** the Examiner asserts that a NETLIST is an ordered list, and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

3.6 As regards **Claim 9** the *Rajgopal et al.* reference discloses simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits, and reporting the results of simulating the non-domino circuits **(Figure 1, Col. 7 Lines 26-39).**

4. **Claims 10, 11, 12, 14, 15, 16 and 17** are rejected under **35 U.S.C. 103(e)** over **Rajgopal et al. U.S. Patent 6,363,515** in view of and in further view of **Beausang U.S. Patent 5,828,579** and in further view of **Conn et al. U.S. Patent 5,999,714.**

4.1 As regards independent **Claims 10, 15 and 17** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and**

Col. 4 Lines 1-22), and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation to combine)* the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

4.2 As regards **Claim 10** the *Rajgopal et al.* reference does not expressly disclose a machine readable medium.

The *Conn et al.* reference discloses a machine readable medium **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.3 As regards **Claim 15** the *Rajgopal et al.* reference does not expressly disclose a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller.

The *Conn et al.* reference discloses a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.4 As regards **Claim 17** the *Rajgopal et al.* reference does not expressly disclose an apparatus.

The *Conn et al.* reference discloses an apparatus **(Col. 2 Lines 22-42).**
It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and

performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.5 As regards **Claims 11 and 16** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

4.6 As regards to **Claim 12** the *Rajgopal et al.* reference discloses reporting results **(Figure 1, Col. 7 Lines 26-39).**

4.7 As regards **Claim 14** the *Rajgopal et al.* reference discloses an ordered list **(Figure 6 Item 72, Figure 5 "Block Netlist for Adder")** the Examiner asserts that a NETLIST is an ordered list. The *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item 22),** and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

5. **Claims 18 and 20** are rejected under **35 U.S.C. 103(e)** as being unpatentable over **Rajgopal et al. U.S. Patent 6,363,515** in view of **Beausang U.S. Patent 5,828,579** and in further view of **Srivastava et al. U.S.Patent 6,344,759.**

5.1 As regards independent **Claim 1** and dependent **Claim 3** see the rejections in paragraph **3** above.

5.2 As regards independent **Claim 4** and dependent **Claims 5 and 6** see the rejections in paragraph **3** above.

5.3 As regards **Claim 18 and 20** the *Rajgopal et al.* reference does not expressly disclose reporting a worst-case noise condition for a simulated domino circuit.

The *Srivastava et al.* reference discloses reporting a worst case noise condition for a simulated domino circuit **(Col. 1 Lines 40-65).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Srivastava et al.* reference because *(motivation to combine)* the invention disclosed in the *Srivastava et al.* reference is useful in domino circuits ***(Srivastava et al. Col. 2 Lines 50).***

Allowable Subject Matter

6. **Claims 19, 21, 22, 23, 24, 25, 26 and 27** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7.

7.1 The Applicant has changed to scope of the original claims and, in light of an updated search, the Examiner has applied new art rejections to Applicant's amended claims.

7.2 In view of Applicant's Request for Continued Prosecution this action is made **NON-FINAL.**

7.3 Claims 19, 21, 22, 23, 24, 25, 26 and 27 are objected to because they are dependent on rejected base Claims.

7.4 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
March 20, 2003

Russell Frejd

RUSSELL FREJD
PRIMARY EXAMINER

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability Extensions of time may NOT be obtained under the provisions of 37 CFR 1 136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in ABANDONMENT of the application.